CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A semiconductor die package, comprising:

a flexible substrate having first and second surfaces;

a first support frame associated with at least one of said first and second surfaces for supporting said flexible substrate, said first support frame defining a cavity;

a semiconductor die containing an array of pixels positioned within said cavity, said semiconductor die supported by said flexible substrate;

a lens structure having an optical path to said array of pixels on said semiconductor die; and

a second support frame associated with the other of said first and second surfaces.

2. The semiconductor die package of claim 1, wherein said second support frame defines a cavity.

3. The semiconductor die package of claim 2, wherein said cavity defined by said second support frame is substantially aligned with said cavity defined by said first support frame.

4. The semiconductor die package of claim 2, further comprising a rigid structure positioned within said cavity defined by said second support frame

5. The semiconductor die package of claim 4, wherein said rigid structure includes a heat conductive element.

6. The semiconductor die package of claim 1, wherein said first and second support frames are coupled to each other through holes formed within said flexible substrate.

7. The semiconductor die package of claim 1, wherein said flexible substrate is an elastomeric substrate.

8. The semiconductor die package of claim 7, wherein said elastomeric substrate is selected from a group comprising epoxy, polyimide, and polyester.

9. The semiconductor die package of claim 8, wherein said polyimide comprises DuPont Kapton®.

10. The semiconductor die package of claim 7, wherein said elastomeric substrate is selected from a material capable of withstanding a 180° angle bend at a radius of at least 1/8" or less.

11. The semiconductor die package of claim 7, wherein said elastomeric substrate is selected from a material having a tensile strength of about 10 kpsi or greater, as measured by ASTM D-882-83 Method A.

12. The semiconductor die package of claim 7, wherein said elastomeric substrate is selected from a material having a tensile modulus of about 200 kpsi or greater, as measured by ASTM D-882-83 Method A.

13. The semiconductor die package of claim 7, wherein said elastomeric substrate is selected from a material having an elongation property of about 25% or more, as measured by ASTM D-882-83 Method A.

14. The semiconductor die package of claim 7, wherein said elastomeric substrate has at least one conductive line formed therein.

15. The semiconductor die package of claim 14, wherein said semiconductor die is electrically coupled to said at least one conductive line by wire bonds.

16. The semiconductor die package of claim 14, wherein said semiconductor die is electrically coupled to said at least one conductive line by conductive pads.

17. The semiconductor die package of claim 1, wherein at least one of said first or second surfaces of said flexible substrate has at least one conductive line formed thereon.

18. The semiconductor die package of claim 1, further comprising an infrared lens formed over said semiconductor die.

19. A semiconductor assembly comprising:

a semiconductor die package, said semiconductor die package comprising:

a flexible substrate having first and second surfaces,

a first support frame associated with at least one of said first and second surfaces for supporting said flexible substrate, said first support frame defining a cavity,

a semiconductor die containing an array of pixels supported by said flexible substrate and positioned within said cavity,

a lens structure providing an optical path to said array of pixels, and

a second support frame associated with the other of said first and second surfaces of said flexible substrate; and

an edge connector electrically coupled to said semiconductor die package.

20. The semiconductor assembly of claim 19, wherein said second support frame of said semiconductor die package defines a cavity.

21. The semiconductor assembly of claim 20, wherein said cavity defined by said second support frame is substantially aligned with said cavity defined by said first support frame.

22. The semiconductor assembly of claim 20, wherein said semiconductor die package further comprises a rigid structure within said cavity defined by said second support frame.

23. The semiconductor assembly of claim 22, wherein said rigid structure includes a heat conductive element.

24. The semiconductor assembly of claim 19, wherein said first and second support frames of said semiconductor die package are coupled to each other through holes formed within said flexible substrate.

25. The semiconductor assembly of claim 19, wherein said flexible substrate of said semiconductor die package is an elastomeric substrate.

26. The semiconductor die package of claim 25, wherein said elastomeric substrate is selected from a group comprising epoxy, polyimide, and polyester.

27. The semiconductor die package of claim 25, wherein said polyimide comprises DuPont Kapton®.

28. The semiconductor die package of claim 25, wherein said elastomeric substrate is selected from a material capable of withstanding a 180° angle bend at a radius of at least 1/8" or less.

29. The semiconductor die package of claim 25, wherein said elastomeric substrate is selected from a material having a tensile strength of about 10 kpsi or greater, as measured by ASTM D-882-83 Method A.

30. The semiconductor die package of claim 25, wherein said elastomeric substrate is selected from a material having a tensile modulus of about 200 kpsi or greater, as measured by ASTM D-882-83 Method A.

31. The semiconductor die package of claim 25, wherein said elastomeric substrate is selected from a material having an elongation property of about 25% or more, as measured by ASTM D-882-83 Method A.

32. The semiconductor assembly of claim 25, wherein said elastomeric substrate has at least one conductive line formed therein.

33. The semiconductor assembly of claim 19, wherein said semiconductor die package further comprises a conductive line formed on at least one of said first and second surfaces of said flexible substrate.

34. The semiconductor assembly of claim 19, wherein said semiconductor die package further comprises an infrared lens formed over said semiconductor die.

35. An imaging apparatus comprising:

a processor; and

an image sensing unit having a semiconductor die package and an edge connector electrically coupling said processor and said semiconductor die package, said semiconductor die package comprising:

a flexible substrate having first and second surfaces,

a first support frame associated with at least one of said first and second surfaces for supporting said flexible substrate, said first support frame defining a cavity,

a semiconductor die containing an array of pixels supported by said flexible substrate and positioned within said cavity;

a lens structure providing an optical path to said array of pixels, and

a second support frame associated with the other of said first and second surfaces of said flexible substrate.

36. The imaging apparatus of claim 35, wherein said semiconductor die package further comprises a cavity defined by said second support frame.

37. The imaging apparatus of claim 36, wherein said cavity defined by said second support frame is substantially aligned with said cavity defined by said first support frame.

38. The imaging apparatus of claim 36, wherein said semiconductor die package further comprises a rigid structure within said cavity of said second support frame.

39. The imaging apparatus of claim 38, wherein said rigid structure includes a heat conductive element.

40. The imaging apparatus of claim 35, wherein said first and second support frames of said semiconductor die package are coupled to each other through holes formed within said flexible substrate.

41. The imaging apparatus of claim 35, wherein said flexible substrate of said semiconductor die package is an elastomeric substrate.

42. A method of forming a semiconductor die package, said method comprising the acts of:

forming a first support frame on at least one of first and second surfaces of a flexible substrate, said first support frame defining a cavity;

forming a second support frame on the other of said first and second surfaces of said flexible substrate;

forming a semiconductor die having an array of pixels within said cavity defined by said first support frame; and

forming a lens structure over said semiconductor die, said lens structure having an optical path to said array of pixels.

43. The method of claim 42, further comprising the step of forming a cavity within said second support frame.

44. The method of claim 43, wherein said cavity defined by said second support frame is substantially aligned with said cavity defined by said first support frame.

45. The method of claim 43, further comprising the step of forming a rigid structure within said cavity defined by said second support frame.

46. The method of claim 45, further comprising the step of forming a heat conductive element within said rigid structure.

47. The method of claim 42, wherein said step of forming said first and second support frames further comprises coupling said first and second support frames to each other through holes formed within said elastomeric substrate.

48. The method of claim 42, wherein said flexible substrate is an elastomeric substrate.

49. The method of claim 48, wherein said elastomeric substrate is selected from a group comprising epoxy, polyimide, and polyester.

50. The method of claim 48, wherein said polyimide comprises DuPont Kapton®.

51. The method of claim 48, wherein said elastomeric substrate is selected from a material capable of withstanding a 180° angle bend at a radius of at least 1/8" or less.

52. The method of claim 48, wherein said elastomeric substrate is selected from a material having a tensile strength of about 10 kpsi or greater, as measured by ASTM D-882-83 Method A.

53. The method of claim 48, wherein said elastomeric substrate is selected from a material having a tensile modulus of about 200 kpsi or greater, as measured by ASTM D-882-83 Method A.

54. The method of claim 48, wherein said elastomeric substrate is selected from a material having an elongation property of about 25% or more, as measured by ASTM D-882-83 Method A.

55. The method of claim 48, further comprising the step of forming at least one conductive line within said elastomeric substrate.

56. The method of claim 55, further comprising the step of electrically coupling said semiconductor die with said at least one conductive line by wire bonds.

57. The method of claim 55, further comprising the step of electrically coupling said semiconductor die with said at least one conductive line by conductive pads.

58. The method of claim 42, further comprising the step of forming an infrared lens over said semiconductor die.